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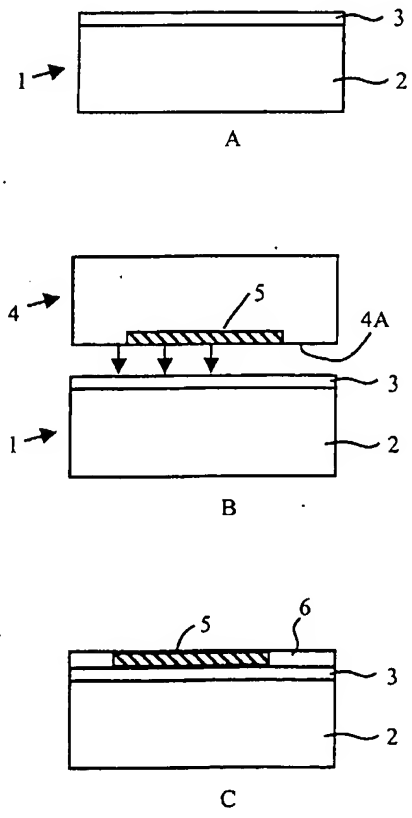
(54) Title: INTEGRATED OPTICAL DEVICES



(57) Abstract: A method of fabricating an integrated optical device comprising an optically conductive layer (6) separated from a substrate (2) by an optical confinement layer (3) comprising the steps of: forming the device by bonding two separate parts (1, 4) together at an interface (4A) therebetween; and forming a first feature (5) at the interface (4A) by processing at least one (4) of the two parts before the two parts (1, 4) are bonded together. The method is particularly applicable to fabricating devices in silicon-on-insulator with the feature (5) located away from the outer surface thereof. The method also allows for the two parts (1, 4) to be bonded together in different crystallographic orientations.

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INTEGRATED OPTICAL DEVICES

TECHNICAL FIELD OF THE INVENTION

This invention relates to a method of fabricating integrated optical devices and, in particular, devices comprising a layer of silicon separated from a substrate by an insulating layer and to devices fabricated by the method.

BACKGROUND TO THE INVENTION

It is known to fabricate a silicon-on-insulator (SOI) wafer for use in microelectronics or for integrated optics by forming an oxide layer within a silicon substrate and then forming a silicon layer over the oxide layer, e.g. by epitaxial growth. Features of the electronic and/or optical circuit are then fabricated in the upper silicon layer.

With the increasing use of SOI wafers for integrated optics, and the increased complexity of such devices, it would be desirable to provide other ways of fabricating the devices.

SUMMARY OF THE INVENTION

According to a first aspect of the invention, there is provided a method of fabricating an integrated optical device comprising an optically conductive layer separated from a substrate by an optical confinement layer comprising the steps of:

forming the device by bonding two separate parts together at an interface therebetween; and

forming a first feature at the interface by processing at least one of the two parts before the two parts are bonded together.

According to another aspect of the invention, there is provided an integrated optical device on a silicon-on-insulator chip fabricated by such a method.

According to a further aspect of the invention, there is provided an integrated optical device comprising an optically conductive layer separated from substrate by an optical confinement layer, the device having been formed from two parts bonded together at an interface, a first feature being provided at the interface by processing at least one of the two parts before the two parts are bonded together.

According to yet a further aspect of this invention, there is provided an integrated optical device fabricated by bonding together two wherein the two parts are bonded together at different crystallographic orientations. Bonding together two parts provides greater flexibility in the fabrication of an optical device as features can be formed in each part independently of features in the other part. One particular aspect of this is the crystallographic orientation of the two parts.

Preferred and optional features of the invention will be apparent from the following description and from the subsidiary claims of the specification.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will now be further described, merely by way of example, with reference to the accompanying drawings, in which:

Figures 1A-1C are schematic diagrams illustrating steps of one embodiment of a method according to the present invention;

Figures 2A-2C, 3A-3C and 4A-4C are schematic drawings illustrating further embodiments of methods according to the present invention;

Figures 5 and 6 are schematic side views of two types of device that may be formed by such methods; and

Figure 7 is a perspective view of two wafers being bonded together at different crystallographic orientations.

BEST MODE OF THE INVENTION

Figure 1A shows a first wafer 1 comprising a substrate 2, e.g. of silicon, with a layer 3 of oxide, e.g. silicon dioxide, on the surface thereof. A native oxide layer forms on silicon when exposed to air or any other oxygen containing environment and the thickness of this may be increased, e.g. to around 0.4-0.5 microns, by thermal oxidation.

Figure 1B shows a second wafer 4 formed of silicon. The second wafer 4 has been processed to form a feature on one face 4A thereof as indicated by the shaded region 5. The face 4A is then bonded to the oxide layer 3 of the first wafer 1 as indicated in the Figure.

A preferred bonding technique is known as direct wafer bonding (DWB). Direct wafer bonding generally involves preparation of the surfaces to be bonded to make them as smooth as possible and pressing the two surfaces together. Some form of thermal cycling may also be used to increase the bond strength. Once such process comprises the steps of:

a) immersing the two wafers 1, 4 in a bath of fluid so as to form OH bonds between the two wafers,
b) applying pressure to force the two wafers 1, 4 together, and
c) applying heat to draw H_2O away from the interface between the two wafers so the two wafers are held together by inter-atomic forces, e.g. van der Waals' forces.

Such bonding techniques are well known so will not be described further. Such techniques are capable of forming a very strong bond between two parts such that

the interface is no longer detectable and the two parts have, in effect, become one. Other bonding techniques providing a similar result may also be used.

After the two wafers have been bonded together, the silicon layer 6 formed by the second wafer 4 may be further processed, e.g. to reduce its thickness, form further features therein and/or polish its surface. Figure 1C illustrates a case in which the thickness of the silicon layer 6 has been reduced until the feature 5 is exposed on the outer surface of the layer 6.

The device illustrated in Figure 1C could, in some cases, be fabricated in the conventional manner, i.e. by processing a silicon-on-insulator chip from the outer surface of the silicon layer but, as will be explained further below, the method described above enables features or devices to be formed which would be impossible, or very difficult, to form by conventional methods and/or which can be formed more easily or with greater accuracy than is possible by conventional methods. For instance, it will be appreciated that if the silicon layer 6 is not reduced in thickness to the extent shown in Figure 1C, the feature 5 will be buried in the silicon layer 6, i.e. beneath the surface thereof. Such buried features are difficult to fabricate by conventional methods.

The feature 5 may take many forms. In one form, it may comprise a hole or recess which, in the final product contains a fluid, either a gas or liquid, for example air. In another case, the feature 5 may be a doped region. In a further case, it may comprise some other material e.g. a polymer or different semi-conductor material, or any combination of the above.

The feature 5 may also take many shapes (and need not be a simple rectangular shape as shown) depending on the nature of the component to be formed thereby.

Figures 2A-2C illustrate the steps of a method in which the first wafer 1 is processed to form a feature on a surface 1A thereof as indicated by the shaded region 7 in Figure 2A. A silicon wafer 4 is then bonded to the surface 1A as illustrated in Figure

2B. The thickness of the silicon layer 6 formed by the wafer 4 may then be reduced, as shown in Figure 2C. Thus, in this case, a feature is pre-formed in the first wafer 3, which carries the oxide layer 3, before the two wafers are bonded together.

The feature 5 may be formed in just the oxide layer 3 and/or may be formed in the substrate 2 beneath the oxide layer 3 as shown in Figure 2.

Features may also be pre-formed in both of the two wafers 1, 4 prior to the wafers being bonded together. In some cases, the features in the respective wafers may be designed to be aligned with each other but in other cases this may not be so and they may be independent of each other.

Features 1 and 2 illustrate a method in which the interface between the two parts being bonded together is between the oxide layer 3 and the silicon layer 6. However, the interface may be at other positions within the device.

Figures 3A to 3C illustrate a method in which the interface is within the silicon layer. An SOI wafer 8 (which may be fabricated by forming an oxide layer 9 on the substrate 10 and then growing an epitaxial layer of silicon 11 on the oxide layer 9 or by forming an oxide layer 9 on the substrate 10, bonding a silicon wafer to the oxide layer and reducing this silicon layer 11 to the required thickness) is processed to form a feature 12 in the surface 11A of the silicon layer 11 as shown in Fig 3A.

A second silicon wafer 13 is then bonded to the surface 11A of the silicon layer 11 of the first wafer. The second silicon wafer 13 may also be processed to form a feature 14 in the surface 13A thereof prior to the surfaces 11A and 13A being bonded together.

Once the two wafers have been bonded together, the thickness of the silicon layer 15 formed by the combination of the silicon layer 11 and wafer 13 is reduced to the required level. The features 12 and 14 are thus formed within the silicon layer 15 as shown in Figure 3C.

It will be appreciated that a feature need not be formed in both wafers prior to bonding but in only one of the wafers, either layer 11 or wafer 13. The feature(s) may also, if desired, extend to the oxide layer 9 and/or to the surface 15A of the silicon layer 15.

Figures 4A to 4C illustrate a method in which the interface is between the substrate and the oxide layer. A silicon wafer 16 is processed to form a feature 17 in a surface 16A thereof as shown in Figure 4A. A second silicon wafer 18 with an oxide layer 19 formed thereon is then bonded to the surface 16A of the first wafer as shown in Figure 4B. Once the two wafers have been bonded together, the thickness of the silicon layer 20 formed by the second wafer 18 is reduced to the required level. The feature 17 is thus formed in the substrate 16 beneath the oxide layer 19.

The feature 17 may, if desired, extend from the oxide layer 19 to the underside 16A of the substrate.

A further feature may, if desired, be formed in the surface of the second wafer 18 bonded to the first wafer 16 prior to bonding the wafers together.

Other features may be formed in the silicon layer 20 before and/or after the two wafers are bonded together.

In all the cases described above, the feature(s) formed in the wafer(s) prior to bonding may take a variety of forms. As mentioned, they may comprise one or more holes or recesses etched into the surface which are filled with air or some other fluid to define one or more components in the silicon layer. They may also comprise doped areas or areas where another material, e.g. polymer or a different semi-conductor material, has been deposited or they may comprise any combination of such elements.

Such holes or recesses may thus be filled with material of a different refractive index than the surrounding material and, each hole or a plurality of holes may be shaped or configured to act as an optical component, e.g. a lens or prism. Alternatively, the holes may define an optical component in the remaining areas of material therebetween or the holes and the remaining material may together form an optical component.

A significant advantage of the methods described is that different parts of an optical device may be fabricated independently of each other, i.e. the processing steps used to fabricate features in one wafer can be carried out entirely independently of processing steps used to fabricate features in the other wafer before the two wafers are bonded together. This increases the choice of processing techniques which may be used in each case and, in particular, enables each of the features to be fabricated to a degree of accuracy greater than would normally be possible if the features were all fabricated on a single wafer.

As indicated above, the features pre-formed on the wafers prior to bonding the wafers together may be buried within the final device. However, they may also be formed so as to extend to an outer surface of the optically conductive layer and/or of the substrate or the thickness of the optically conductive layer and/or the substrate may be reduced until the feature is accessible from an outer surface thereof. Alternatively, or additionally, the optically conductive layer and/or the substrate may be processed after the wafers have been bonded together to provide one or more connections between an outer surface of the device and one or more features buried therein. Such a connection may comprise an optical and/or on an electrical connection and may take a variety of forms. It may, for instance, comprise one or more holes or recesses (filed with air or some other fluid) etched in the device, doped areas or areas filled or partially filled with other material or any combination thereof.

The methods described above can be used to form a wide variety of devices which will not be discussed here although some basic devices or elements which may be formed in this way will be described below.

The feature formed at the interface between the two bonded wafers may, for example comprise a waveguide, e.g. extending in a direction substantially parallel to the plane of the interface.

Figure 5 shows a schematic side view of a waveguide 21 formed in a silicon layer 22 separated from a substrate 23 by an oxide layer 24.

The waveguide 21 may comprise an elongate region having a refractive index differing from that of the surrounding material, e.g. a doped region or a region of different material to the surrounding material, or an elongate region one or more sides of which are defined by elongate holes or channels within the material.

A hole or recess may also be formed in the silicon layer 22 with a reflective facet 25 positioned to re-direct light received from the waveguide 21, in this case out of the chip or to a component (not shown) on the surface of the chip. The hole or recess may also be elongate, e.g. in the form of a trench, and arranged to re-direct light received from a plurality of waveguides.

In another arrangement, the features formed at the interface between the two bonded wafers may have a periodic structure so as to act as a grating for receiving light incident upon the device or directing light out of the device.

Figure 6 shows a schematic side view of a waveguide 26 formed in a silicon layer 27 separated from a substrate 28 by an oxide layer 29. Part of the waveguide 26 is formed with a periodic structure 30 as shown. The periodic structure 30 may take many forms which provide a periodicity in the refractive index of the waveguide along its length. It may, for instance, comprise alternating regions of silicon and holes (filled with air or other material) or alternating regions having different dopant levels or any other periodic structure known in the field which can be fabricated by the method described above. As indicated by arrows 31 in Figure 6, light incident upon the chip or from a device (not shown) mounted on the chip, received by the grating

formed by the periodic structure 30 is received by the waveguide 26 and transmitted along the waveguide.

It will be appreciated that both of the devices shown in Figures 5 and 6 can be operated in either direction, i.e. for receiving light into a waveguide in the device or transmitting light from the waveguide in the device.

Figure 7 illustrates a further advantage of fabricating a device by bonding together two parts.

Normally, if an optical device is fabricated from a single wafer, the crystallographic material of the wafer has the same crystallographic orientation throughout. For example, in a silicon-on-insulator (SOI) chip fabricated by implanting an oxide layer within a silicon wafer, the silicon layer above the oxide layer has the same crystallographic orientation as the silicon layer beneath the oxide layer.

However, if two parts are to be bonded together, their relative orientations can be selected prior to bonding the two parts together. In particular, when an SOI wafer is formed by bonding a silicon layer to an oxide layer formed on another silicon layer, the orientations of the two silicon layers can be selected as required.

The fabrication of some features in a crystalline material such as silicon is dependent on the crystallographic orientation of the material, e.g. because wet etch processes tends to follow crystallographic planes within the material or because the accuracy of fabrication is dependent upon crystallographic orientations, e.g. epitaxial growth. Some devices may require features which are preferably formed at different crystallographic orientation but which, nevertheless, need to be formed at specific orientations relative to each other. By constructing a device as described above so that parts thereof are in different crystallographic orientations, it can be arranged that each feature is fabricated at the preferred crystallographic orientation but that the relative orientation of the features can be independently selected.

With devices of the type described above, one or more of the features may be fabricated in the respective parts prior to bonding the parts together, or the features may be fabricated after the parts have been bonded together.

The two parts may be bonded together at any angle relative to each other but, typically, the crystallographic orientations of the two parts may be arranged at 45 degrees or 90 degrees to each other.

Figure 7 shows two silicon wafers 41, 42, each wafer having a flat 41A, 42A which corresponds to a given crystallographic direction, e.g. < 100 > direction. The wafers are bonded together so that flats 41A and 42A are at 45 degrees to other. A first feature 43 which is preferably formed perpendicular to the < 100 > direction is formed in the first wafer 41. A second feature 44 which preferably formed at an angle of 45 degrees to the < 100 > direction is formed in the second wafer 42, yet by bonding the wafers together at 45 degrees to each other, the two features can be fabricated at a selected orientation to each other, in this case parallel to each other. Feature 43 may be a feature formed by wet etching in a silicon substrate formed by wafer 41, whereas feature 44 may be formed by epitaxial growth in an optically conducting layer of silicon formed by wafer 42.

As described above, the fabrication methods described herein are particularly suitable for fabricating optical devices in silicon-on-insulator (SOI) chips. Such chips comprise an optically conductive silicon layer separated from a substrate, which is also usually of silicon, by an insulating layer, such as an oxide, typically silicon dioxide.

The term 'insulating layer' is derived from the initial use of SOI chips for the fabrication of electronic integrated circuits. When such chips are used for fabrication of optical integrated circuits, this layer acts as an optical confinement layer, i.e. it serves to confine optical modes within the optically conductive silicon layer due to it either not being optically conductive or having a higher refractive index than the optically conductive silicon layer.

Whilst the use of silicon as the optically conductive layer and the use of silicon dioxide as the optical confinement layer is preferred, it will be appreciated that the methods described above may also be suitable for fabricating integrated optical circuits in which the optically conductive layer and/or the optical confinement layer are formed of other materials.

The methods described above may also be extended to bond more than two parts together. Two or more parts may, for instance, be bonded side-by-side to the same wafer on three or more parts may be bonded together in a stack. One or more further features may thus be formed at the interface between these parts by processing at least one of the respective parts prior to bonding them together.

CLAIMS

1. A method of fabricating an integrated optical device comprising an optically conductive layer separated from a substrate by an optical confinement layer comprising the steps of:

   forming the device by bonding two separate parts together at an interface therebetween; and

   forming a first feature at the interface by processing at least one of the two parts before the two parts are bonded together.

2. A method as claimed in claim 1 in which the interface is between the optically conductive layer and the optical confinement layer.

3. A method as claimed in claim 1 in which the interface is within the optically conductive layer.

4. A method as claimed in claim 1 in which the interface is between the substrate and the optical confinement layer.

5. A method as claimed in any preceding claim in which the first feature is formed in only one of the parts.

6. A method as claimed in any of claims 1 - 4 in which the first feature comprises a first element in one of the parts and a second element in the other of the parts, the two parts being aligned so the first and second elements are aligned with each other.

7. A method as claimed in any preceding claim in which the first feature comprises a hole filled with fluid.

8. A method as claimed in claim 7 in which the fluid is air.

9. A method as claimed in any preceding claim in which the optically conductive layer and the substrate are formed of a first material or of a first material and a second material respectively, and the first feature comprises a region of a third material which differs from the first and/or the second material.

10. A method as claimed in claim 9 in which the third material differs from the first and/or second materials by virtue of dopant with the said region.

11. A method as claimed in claim 9 or 10 in which the first and/or second materials are semi-conductors and the said region comprises a different semiconductor material.

12. A method as claimed in any preceding claim in which the optically conductive layer is formed of silicon.

13. A method as claimed in any preceding claim in which the optical confinement layer comprises an oxide.

14. A method as claimed in claims 12 and 13 in which the oxide comprises silicon dioxide.

15. A method as claimed in any preceding claim in which the two parts are bonded together by a direct bonding technique.

16. A method as claimed in claim 15 in which the direct bonding technique comprises the steps of:

immersing the two parts in a bath of fluid so as to form OH bonds between the two parts;

applying pressure to force the two parts together; and

applying heat to drive H_2O away from the interface whereby the two parts are held together by van der Waals' forces.

17. A method as claimed in any preceding claim comprising the further step of reducing the thickness of one or both of the two parts after the two parts have been bonded together.

18. A method as claimed in any preceding claim comprising the further step of polishing an outer surface of the optically conductive layer after the two parts have been bonded together.

19. A method as claimed in any preceding claim comprising the further step of fabricating a second feature, before and/or after the two parts are bonded together, in the first and/or second part to provide a connection between the first feature and an outer surface of the device.

20. A method as claimed in any preceding claim in which one or more further parts are bonded to either the first and/or second part at a further interface therebetween, a further feature being formed at the further interface by processing at least one of the respective parts prior to bonding them together.

21. A method of fabricating an integrated optical device substantially as hereinbefore described with reference to one or more or the accompanying drawings.

22. An integrated optical device comprising an optically conductive layer separated from substrate by an optical confinement layer, the device having been formed from two parts bonded together at an interface, a first feature being provided at the interface by processing at least one of the two parts before the two parts are bonded together.

23. A device as claimed in claim 22 in which the first feature is located at a boundary between the layer of optically conductive material and the layer of optical confinement material.

24. A device as claimed in claim 22 in which the first feature is within the layer of optically conductive material.

25. A device as claimed in claim 22 in which the first feature is located at a boundary between the substrate and the layer of optical confinement material.

26. A device as claimed in clam 22, 23 or 24 in which the first feature comprises a hole filled with fluid.

27. A device as claimed in claim 26 in which the fluid is air.

28. A device as claimed in claim 26 or 27 comprising an optical waveguide, a side of the hole providing a reflective face positioned to re-direct light to or from the waveguide.

29. A device as claimed in claimed in any of claims 22 - 27 in which the first feature has a periodic structure so as to act as a grating for receiving light incident upon the device or directing light out of the device.

30. A device as claimed in claimed any of claims 22 - 28 in which the optically conductive layer and the substrate comprise a first material or first and second materials respectively, and the first feature comprises a region of a third material which differs from the first and/or the second material.

31. A device as claimed in claim 30 in which the third material differs from the first and/or second material by virtue of dopant within the said region.

32. A device as claimed in claim 30 or 31 in which the first and/or second materials are semi-conductors and the said region comprises a different semi-conductor material.

33. A device as claimed in any of claims 22 - 32 in which the optically conductive material is silicon.

34. A device as claimed in any of claims 22 to 33 in which the optical confinement material comprises an oxide.

35. A device as claimed in claim 33 and 34 in which the oxide is silicon dioxide.

36. A device as claimed in any of claims 22 to 35 in which the feature comprises an optical waveguide.

37. A device as claimed in any of claims 22 to 36 comprising a second feature which provides a connection between the first feature and an outer surface of the device.

38. A device as claimed in claim 37 in which the second feature comprises an electrical connection.

39. A device as claimed in claim 37 in which the second feature comprises an optical connection.

40. A device as claimed in any of claims 22 – 39 in which the two parts are at different crystallographic orientations.

41. An integrated optical device fabricated by bonding two parts together wherein the two parts are bonded together at different crystallographic orientations.

42. An integrated optical device on a silicon-on-insulator chip fabricated by a method as claimed in any of claims 1 – 21.

43. An integrated optical device substantially as hereinbefore described with reference to and/or as shown in one or more of the accompanying drawings.

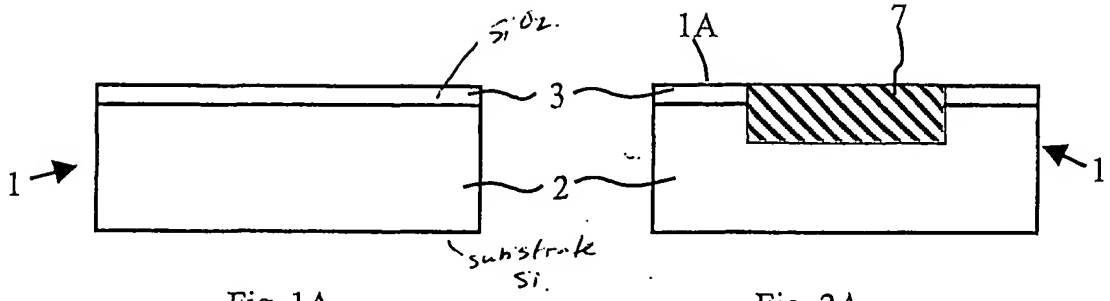

Fig. 1A

Fig. 2A

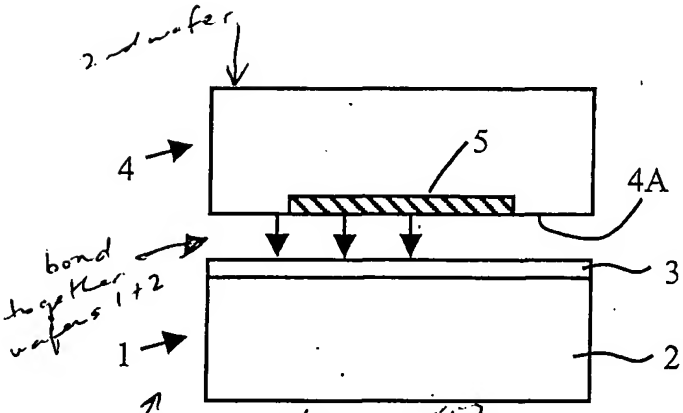

Fig. 1B

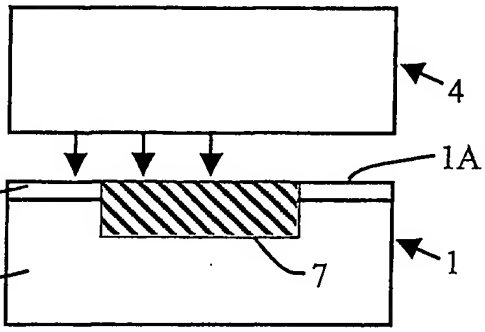

Fig. 2B

- or. immerse press together. in water, heat to draw away H_2O.

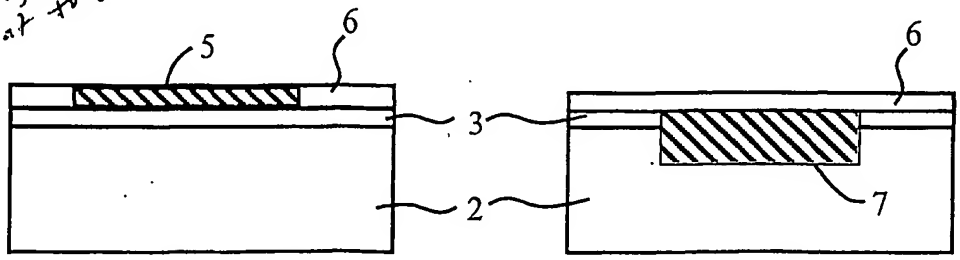

Fig. 1C

Fig. 2C

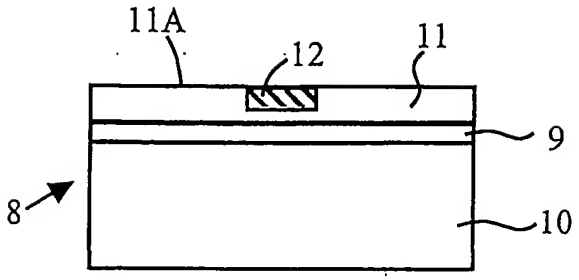

Fig. 3A

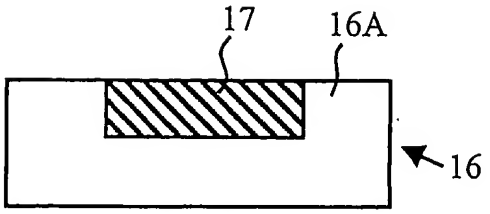

Fig. 4A

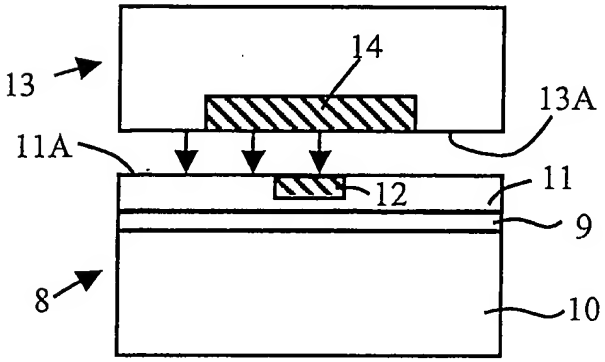

Fig. 3B

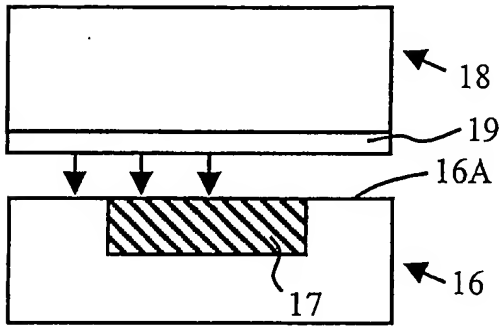

Fig. 4B

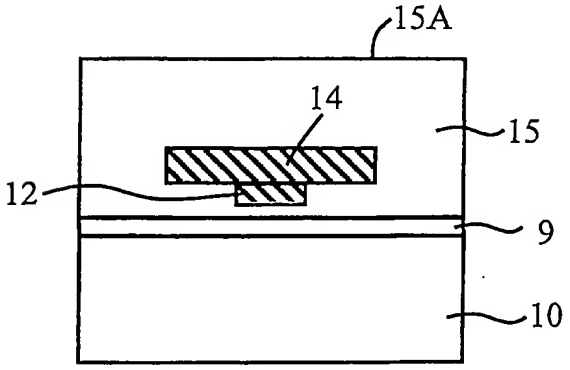

Fig. 3C

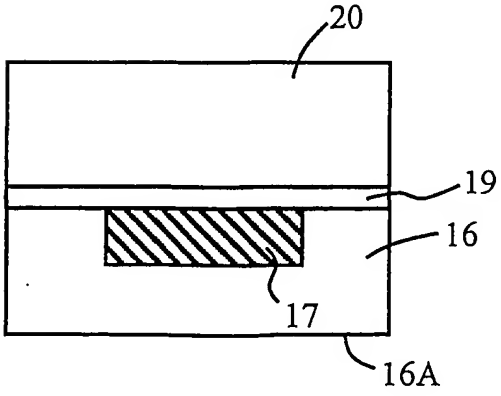

Fig. 4C

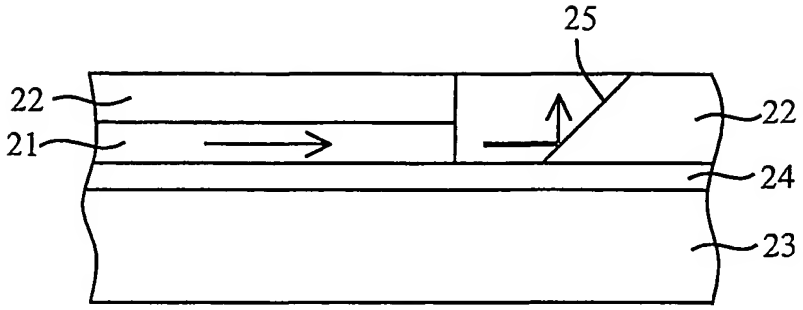

Fig. 5

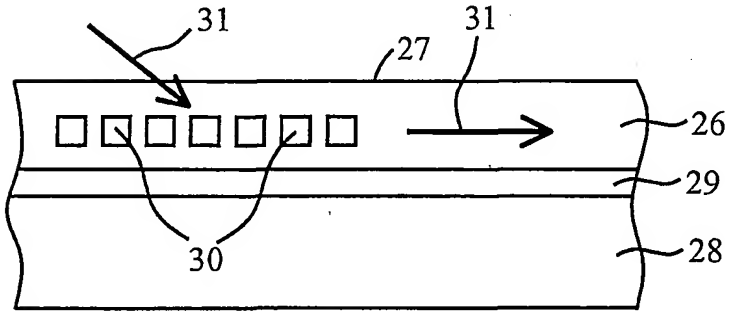

Fig. 6

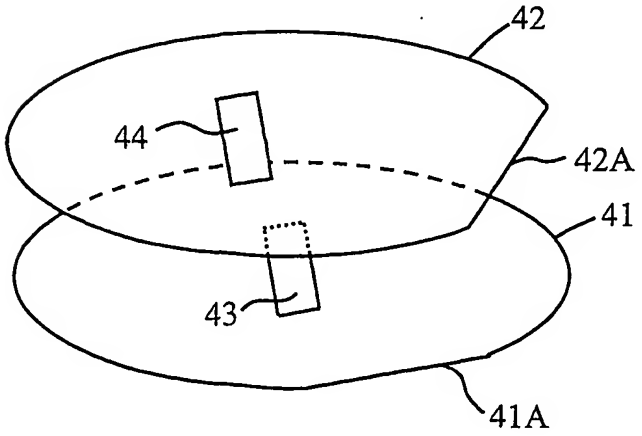

Fig.7

INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 01/05522

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G02B6/13 G02B6/43

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G02B H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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X	CHOUTEAU S ET AL: "OPTOELECTRONIC MICROSWITCH ON SOI BASED STRUCTURE" 1995 IEEE INTERNATIONAL SOI CONFERENCE PROCEEDINGS. TUCSON, OCT. 3 - 5, 1995, PROCEEDINGS OF THE ANNUAL SOS/SOI TECHNOLOGY CONFERENCE. (FROM 1991 PROCEEDINGS OF THE INTERNATIONAL SOI CONFERENCE.) SILICON-ON-INSULATOR TECHNOLOGY AND DEVICES, NEW YORK,, 3 October 1995 (1995-10-03), pages 40-41, XP000590645 ISBN: 0-7803-2548-6	1,2,4-6, 9,11, 13-15, 17,19, 21-23, 25,30, 32, 34-37, 39,42,43
Y	the whole document	1,3, 7-10,12, 15,16, 18,20, 24, 26-29, 31,33,

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
21 February 2002	07/03/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Frisch, A

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